Electronic Version
Stylesheet Version v1.1.1

[SYSTEM AND METHOD OF ANALYZING TIMING EFFECTS OF SPATIAL DISTRIBUTION IN CIRCUITS]

Abstract

Systems and methods are provided for analyzing the timing of circuits, including integrated circuits, by taking into account the location of cells or elements in the paths or logic cones of the circuit. In one embodiment, a bounding region may be defined around cells or elements of interest, and the size of the bounding region may be used to calculate a timing slack variation factor. The size of the bounding region may be adjusted to account for variability in timing delays. In other embodiments, centroids may be calculated using either the location or the delay-weighted location of elements or cells within the path or cone and the centroids used to calculate timing slack variation factor. The timing slack variation factors are used to calculate a new timing slack for the path or logic cone of the circuit.